Abstract

An adder includes a number of computational stages each associated with one or more bit positions. Particular ones of the computational stages generate a sum output signal and a primary carry-output signal of the adder. A flag generation circuit is coupled to at least one of the stages and is operative to generate an overflow flag for the adder substantially in parallel with the generation of the sum output signal and the primary carry-output signal of the adder. Advantageously, the invention substantially reduces the computational delay associated with generation of the overflow flag, relative to that of conventional adders, without requiring an increase in transistor count or circuit area.

09733856.120800